

## 100V N-Channel Enhancement Mode MOSFET

### Description

The AP400N10TLG2 uses advanced **APM-SGT II** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 400A$

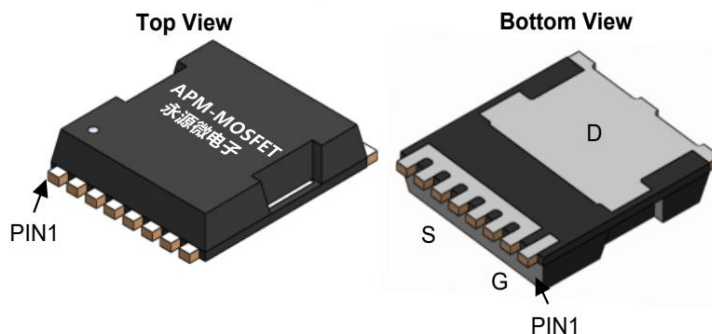
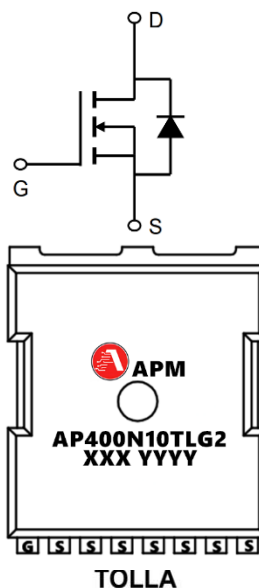
$R_{DS(ON)} < 1.2m\Omega$  @  $V_{GS}=10V$  (Type: **1.0mΩ**)

### Application

DC/DC Converter

LED Backlighting

Power Management Switches



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP400N10TLG2	TOLLA-8L	AP400N10TLG2 XXX YYYY	2000

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	400	A
$I_D @ T_A=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	295	A
IDM	Pulsed Drain Current <sup>2</sup>	1800	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	1987	mJ
IAS	Avalanche Current	50	A
$P_D @ T_A=25^{\circ}C$	Total Power Dissipation <sup>3</sup>	500	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	45	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	0.25	$^{\circ}C/W$

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### Electrical Characteristics ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	$I_D = 250\text{mA}$ , $V_{GS} = 0\text{V}$	100	108	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
IGSS	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$ , $V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{mA}$	2.5	2.9	4.0	V
RDS(ON)	Static Drain-Source ON-Resistance <sup>(4)</sup>	$V_{GS} = 10\text{V}$ , $I_D = 20\text{A}$	-	1.0	1.2	m $\Omega$
R <sub>g</sub>	Gate Resistance	$f = 1\text{MHz}$	-	3.8	-	$\Omega$
C <sub>iss</sub>	Input Capacitance	$V_{GS} = 0\text{V}$ , $V_{DS} = 50\text{V}$ , $f = 1\text{MHz}$	-	13360	-	pF
C <sub>oss</sub>	Output Capacitance		-	5113	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	122	-	pF
Q <sub>g</sub>	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ , $V_{DS} = 50\text{V}$ , $I_D = 20\text{A}$	-	217	-	nC
Q <sub>gs</sub>	Gate Source Charge		-	65	-	nC
Q <sub>gd</sub>	Gate Drain("Miller") Charge		-	57	-	nC
td(on)	Turn-On DelayTime	$V_{GS} = 10\text{V}$ , $V_{DD} = 50\text{V}$ , $I_D = 20\text{A}$ , $R_{GEN} = 3\text{W}$	-	41	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	69	-	ns
td(off)	Turn-Off DelayTime		-	157	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	92	-	ns
IS	Maximum Continuous Body Diode Forward Current		-	-	400	A
ISM	Maximum Pulsed Body Diode Forward Current		-	-	1800	A
VSD	Body Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_S = 20\text{A}$	-		1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 20\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$	93	130	176	ns
Qrr	Body Diode Reverse Recovery Charge		-	374	-	nC

#### Notes:

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is  $V_{DD}=90\text{V}$ ,  $V_{GS}=10\text{V}$ ,  $L=1.0\text{mH}$ ,  $I_{AS}=50\text{A}$
- 4、The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 5、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

### Typical Characteristics

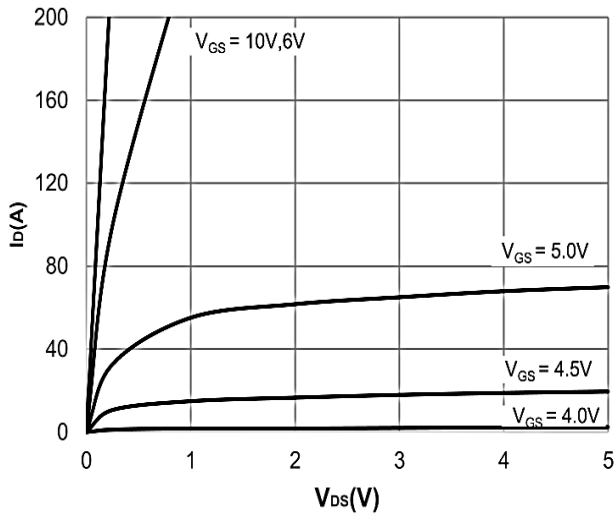


Figure 1: Output Characteristics

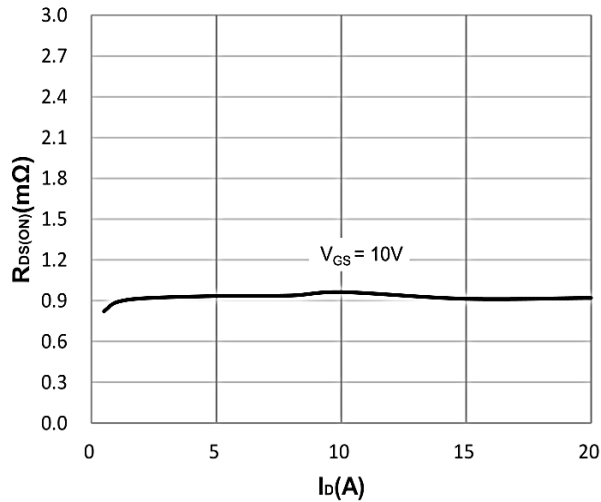


Figure 3: On-resistance vs. Drain Current

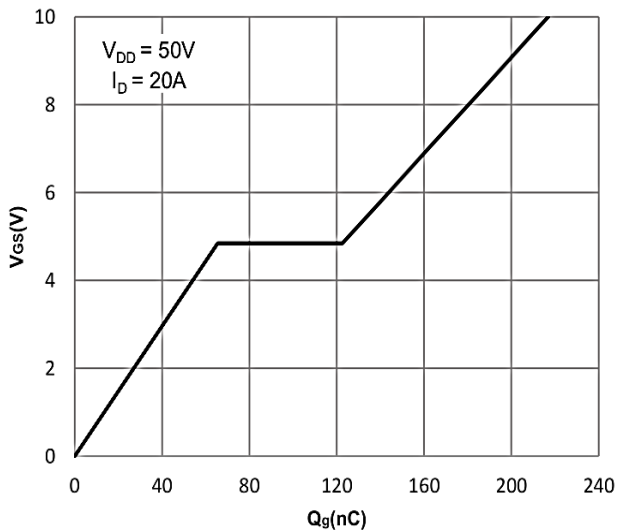


Figure 5: Gate Charge Characteristics

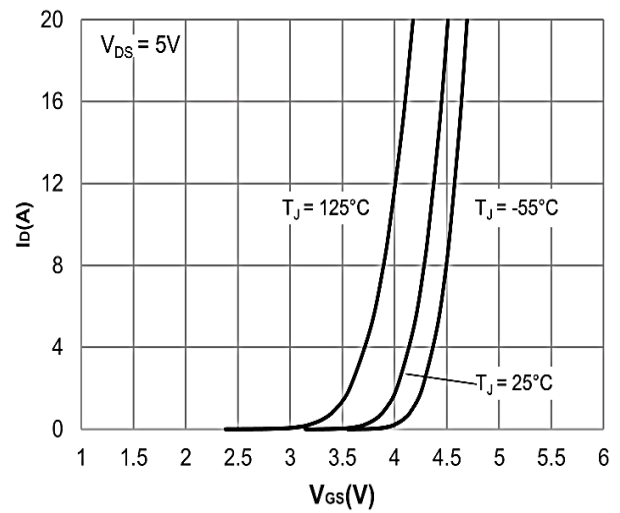


Figure 2: Typical Transfer Characteristics

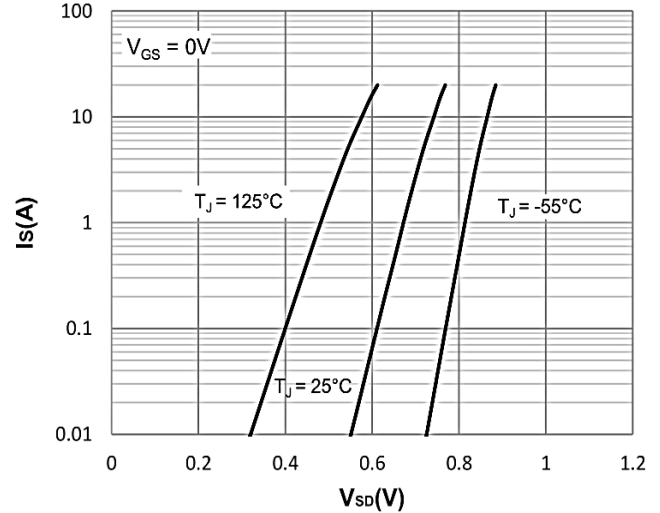


Figure 4: Body Diode Characteristics

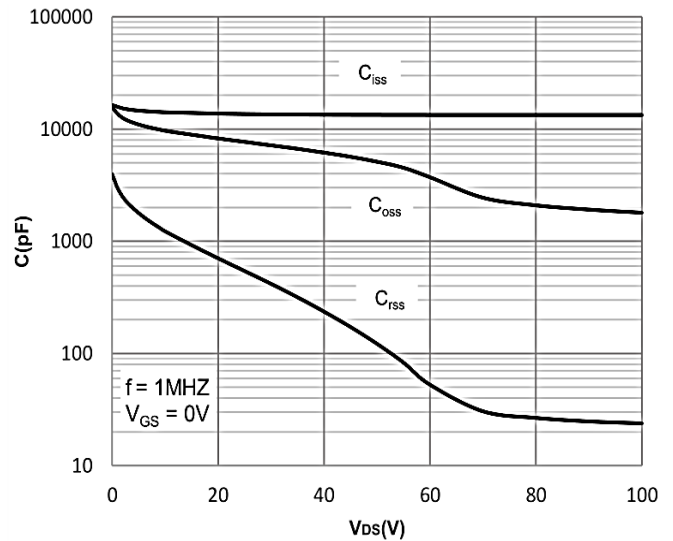


Figure 6: Capacitance Characteristics

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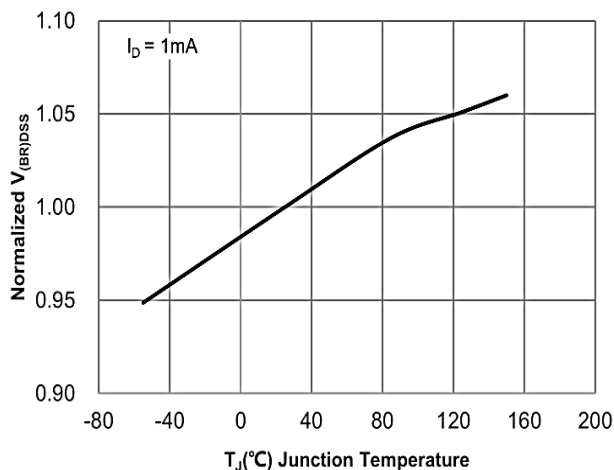


Figure 7: Normalized Breakdown voltage vs.

Junction Temperature

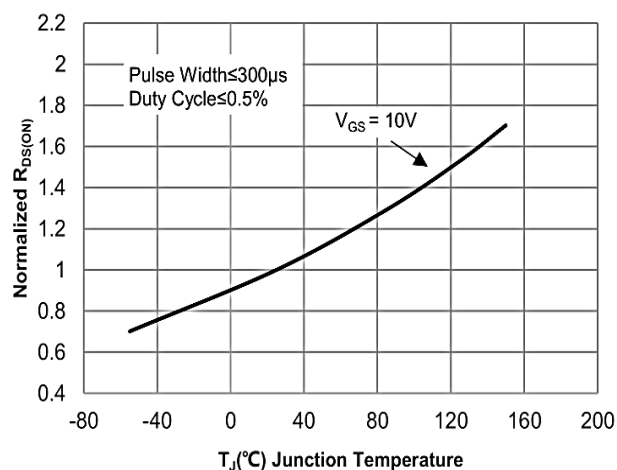


Figure 8: Normalized on Resistance vs.

Junction Temperature

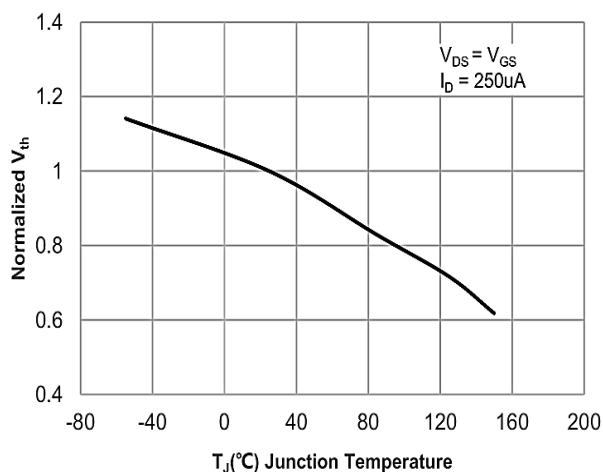


Figure 9: Maximum Safe Operating Area

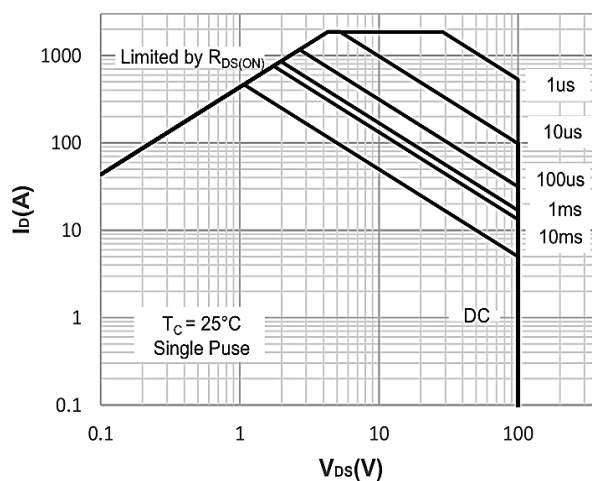


Figure 10: Maximum Continuous Drain Current  
vs. Case Temperature

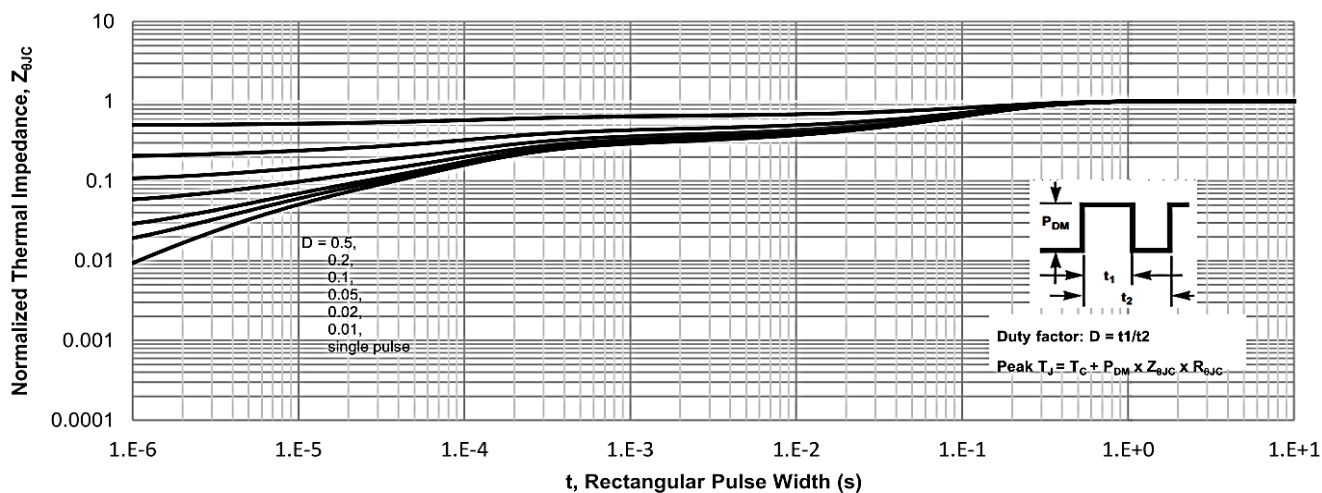
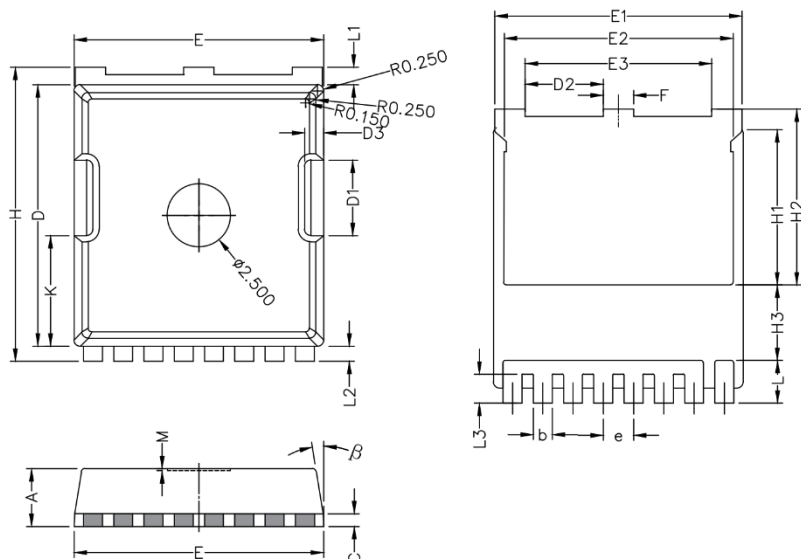


Figure 11: Normalized Maximum Transient Thermal Impedance

### Package Mechanical Data-TOLLA-8L



Symbol	Dim in mm		
	Min	Tpy	Max
A	2.20	2.30	2.40
b	0.65	0.75	0.85
C	0.508REF		
D	10.25	10.40	10.55
D1	2.85	3.00	3.15
D2	2.95	3.10	3.25
D3	0.75REF		
E	9.75	9.90	10.05
E1	9.65	9.80	9.95
E2	8.95	9.10	9.25
E3	7.23	7.40	7.55
e	1.20BSC		
F	1.05	1.20	1.35
H	11.55	11.70	11.85
H1	6.03	6.18	6.33
H2	6.85	7.00	7.15
H3	3.00 BSC		
L	1.55	1.70	1.85
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
β	8°	10°	12°
M	0.08REF		
K	4.25	4.40	4.55

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Edition	Date	Change
REV1.0	2024/5/5	Initial release

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