

Features

- Very Low On-resistance $R_{DS(ON)}$
- Low C_{rss}
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

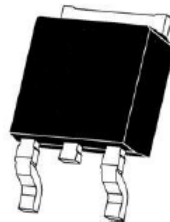
Product Summary



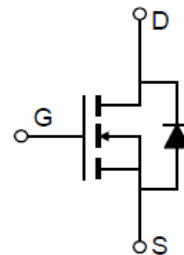
V_{DS}	30	V
$R_{DS(on), Typ@ V_{GS}=10 V}$	2.6	mΩ
I_D	120	A

Application

- PWM Application
- Load Switch
- Power Management



TO-252-2L top view



Schematic diagram

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	30N120KQ	Units
V_{DSS}	Drain-Source Voltage	30	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	120	A
	- Continuous ($T_C = 100^\circ\text{C}$)	78	A
I_{DM}	Drain Current - Pulsed (Note 1)	480	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	156	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	89	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ\text{C/W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	--	2.6	3.1	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	--	3.5	4.5	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	3573	-	pF
C_{oss}	Output Capacitance		--	390	-	pF
C_{rss}	Reverse Transfer Capacitance		--	353	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $R_L = 3\Omega, I_D = 30\text{ A}$ (Note 3)	--	14	--	ns
t_r	Turn-On Rise Time		--	18	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	--	ns
t_f	Turn-Off Fall Time		--	12	--	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 30\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3)	--	72	--	nC
Q_{gs}	Gate-Source Charge		--	46	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC

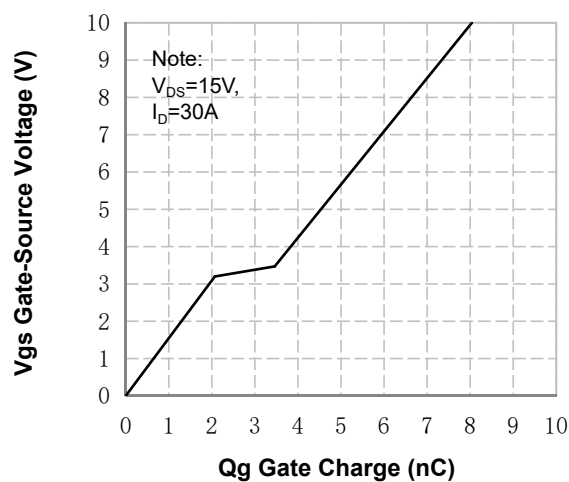
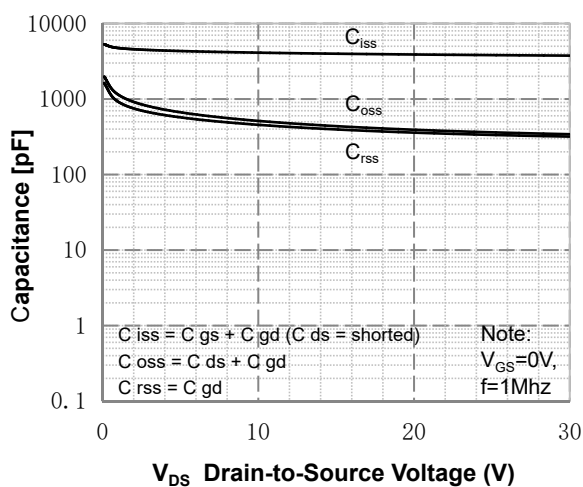
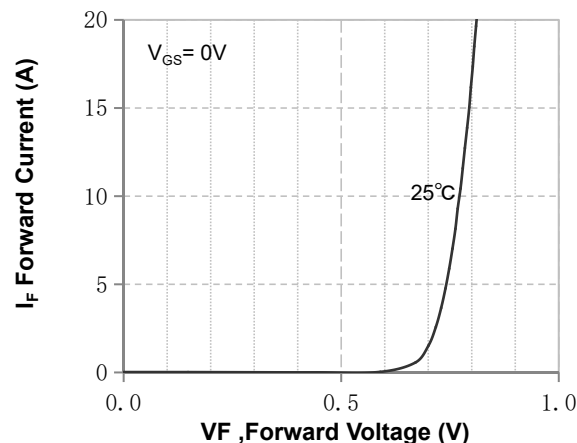
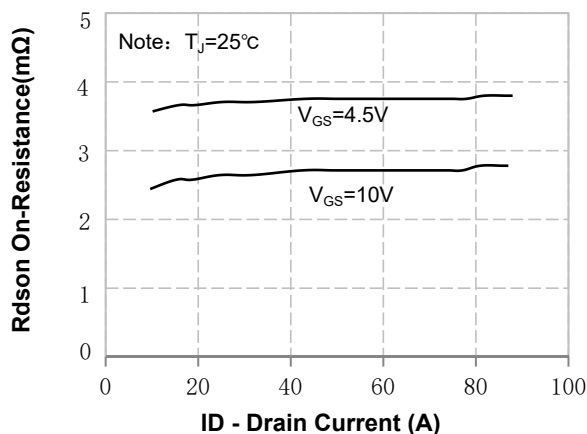
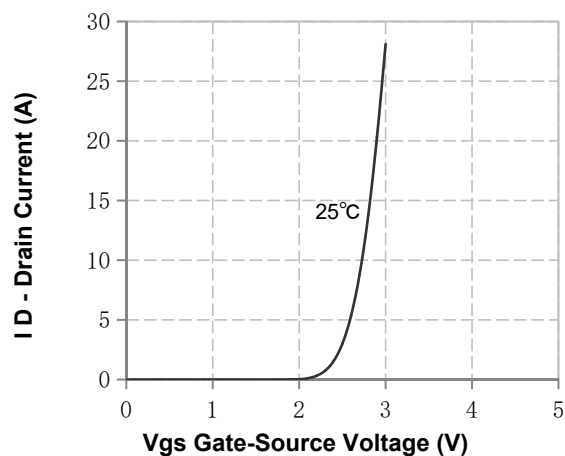
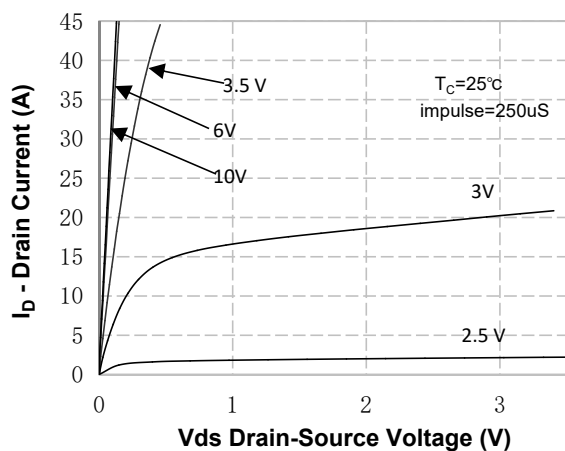
Drain Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	120	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	480	A
V_{SD}	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = 30\text{ A}, T_J = 25^\circ\text{C}$	--	0.7	1.2	V
T_{rr}	Reverse recovery time, $I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		48		ns
Q_{rr}	Reverse recovery charge, $I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		80		nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ\text{C}, V_{DD} = 15\text{ V}, V_G = 10\text{ V}, R_G = 25\Omega, L = 0.5\text{ mH}, I_{AS} = 25\text{ A}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

N- Channel Typical Characteristics



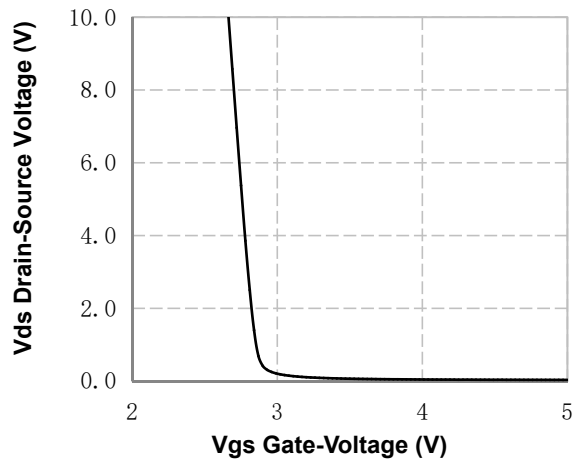
N- Channel Typical Characteristics (Continued)


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

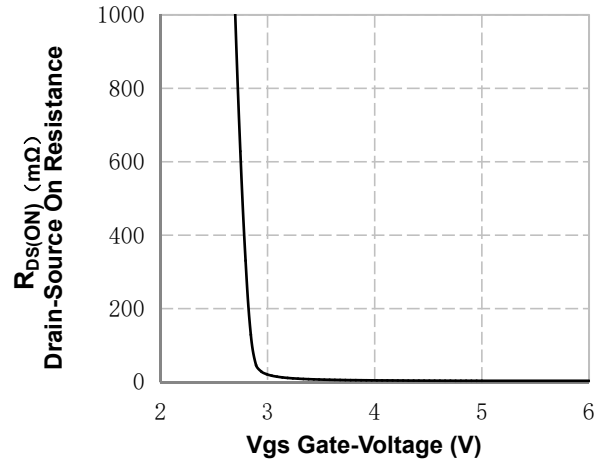


Figure 8. On-Resistance vs Gate Voltage

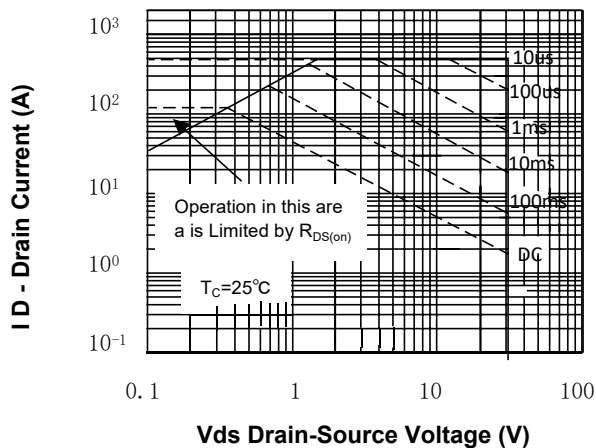


Figure 9. Maximum Safe Operating Area

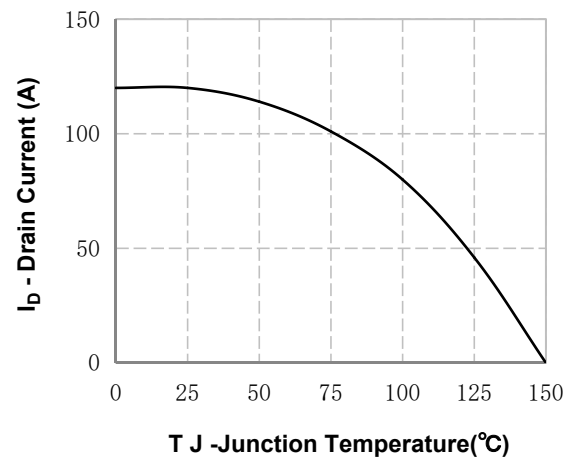


Figure 10. Maximum Continuous Drain Current vs Temperature

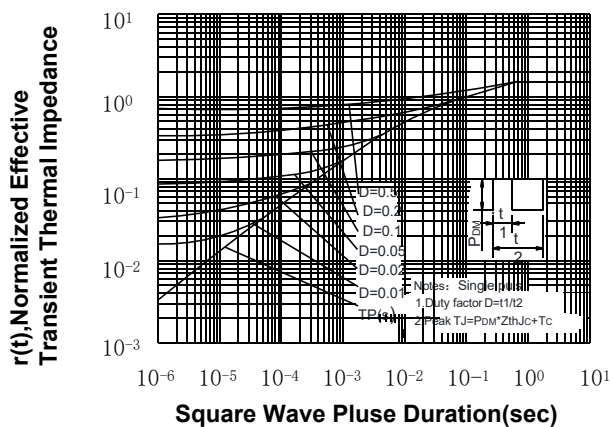
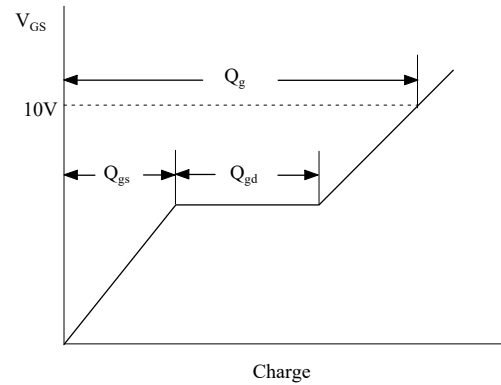
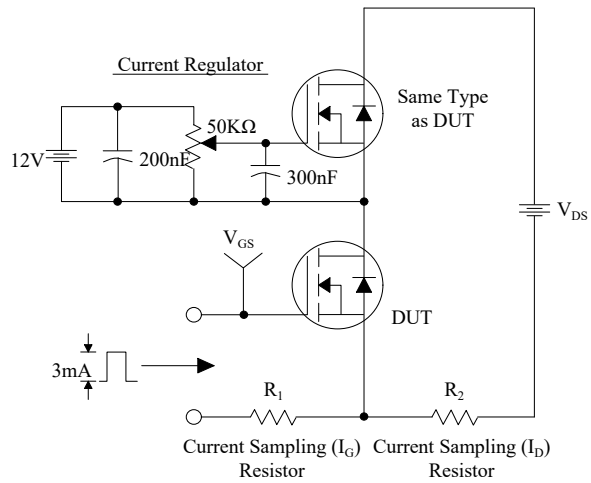
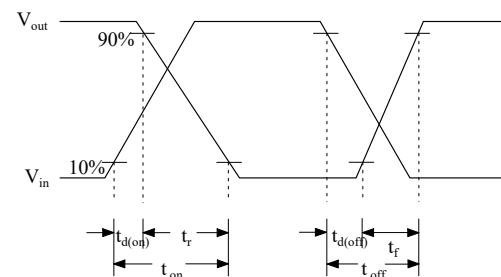
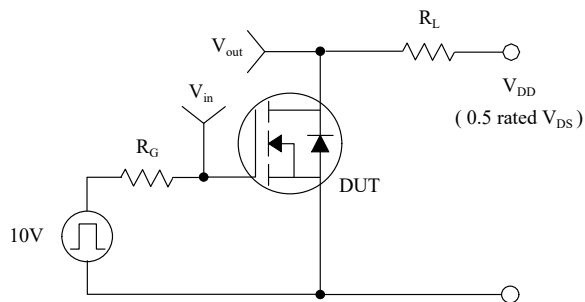


Figure 11. Transient Thermal Response Curve

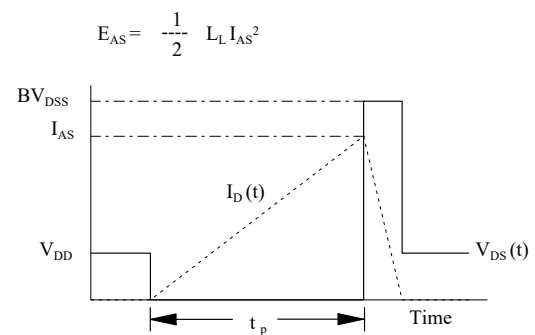
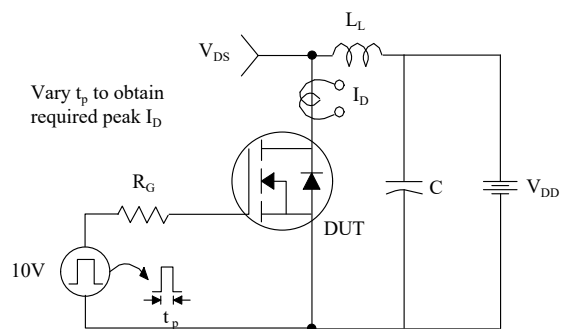
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



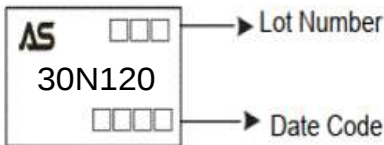
The diagram shows a switching circuit. A Driver MOSFET, labeled "Same Type as DUT", has its gate connected to a voltage source V_{GS} through a resistor R_G . The source of the driver is connected to ground. The drain of the driver is connected to the source of the DUT MOSFET. The DUT MOSFET has its gate connected to a voltage source V_{GS} through a resistor R_G . The drain of the DUT is connected to a load inductor L , which is then connected to a DC supply V_{DD} . The source of the DUT is connected to ground. The current through the DUT is labeled I_s . The voltage across the DUT is labeled V_{DS} . The circuit is controlled by a pulse source V_{GS} .

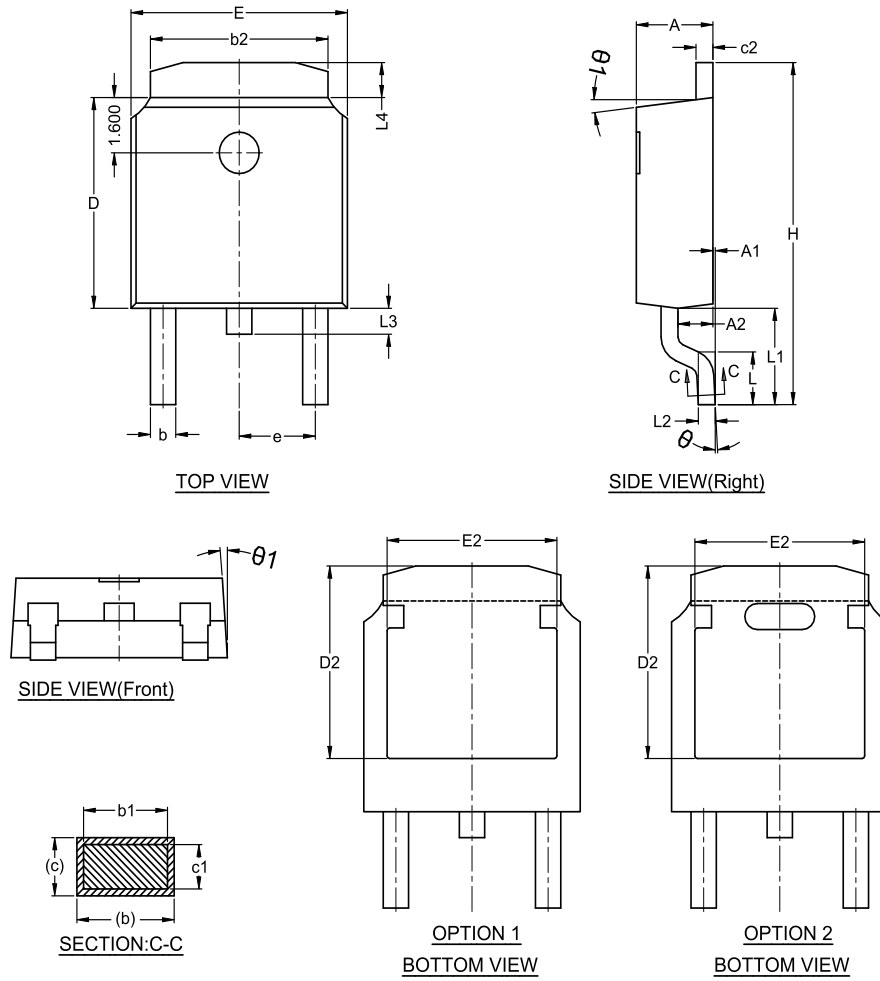
- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM30N120KQ-R	30N120	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 The diagram shows a TO-252 package with the following markings: - Top left: AS (ASDsemi logo) - Top right: (Lot Number) - Middle: 30N120 - Bottom: (Date Code)

TO-252 PACKAGE IN FORMATION


DIM SYMBOL	MIN.	NOM.	MAX.
A	2.200	2.300	2.400
A1	0.000	0.070	0.130
A2	0.950	1.050	1.150
b	0.700	0.800	0.900
b1	0.660	0.760	0.860
b2	5.134	5.334	5.534
c	0.448	0.548	0.648
c1	0.458	0.508	0.558
c2	0.448	0.548	0.648
D	6.000	6.100	6.200
D2	5.372	5.572	5.772
E	6.400	6.500	6.600
E2	4.900	5.100	5.300
e	2.286 BSC.		
H	9.700	9.900	10.100
L	1.380	1.525	1.725
L1	2.588	2.788	2.988
L2	0.508 BSC.		
L3	0.600	0.750	0.950
L4	0.812	1.012	1.212
θ	1°	3°	5°
θ 1	6°	7°	8°

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